



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/073,314

02/13/2002

Kenji Hoshi

020171

4466

38834

7590

04/10/2008

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 CONNECTICUT AVENUE, NW
SUITE 700
WASHINGTON, DC 20036

EXAMINER

MOVVA, AMAR

ART UNIT

PAPER NUMBER

2891

MAIL DATE

DELIVERY MODE

04/10/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/073,314	Applicant(s) HOSHI ET AL.	
	Examiner AMAR MOVVA	Art Unit 2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 January 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4, 13, 15 and 16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 13, 15 and 16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

1. Claims 1-4 ,13 and 15-16 objected to because of the following informalities: The claim limitations of "a device pattern" should be changed to "an element region pattern". The term device has already been used to refer to a semiconductor device as a whole in the preamble of the claims and further in the specification. Nowhere in applicant's specification does "device" refer to the memory region. Furthermore paragraph 2, pg. 9 defines the memory region as being the "element region" . Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4 and 13 and 15-16 are rejected under 35 U.S.C. 102(a) or (e) as being anticipated by Ghinovker '833.

a. Regarding claims 1-4, Ghinovker discloses a semiconductor device comprising a plurality of alignment marks (76, fig. 2-5b) formed over a

semiconductor wafer (lines 40-50, col. 4), each of the alignment marks comprising a micronized pattern (78 of 76, fig. 2-5b), the micronized pattern having a size smaller than a resolution limit of an alignment sensor of field image alignment detecting positions of the alignment marks (fig. 2-5b), the micronized pattern having a pattern forming margin larger than a pattern forming margin which a device pattern formed over the semiconductor wafer has (lines 60-68, col. 4), and wherein all of the alignment marks formed in the entire alignment mark area have the same shape so as to generate about the same field image alignment signal (fig. 2-5b). The micronized pattern is a line-and-space pattern (fig. 2-5b). Each of lines constituting the line-and-space pattern are divided into a broken line having a plurality of segments (78 of 76, fig. 2-5b). Positions of the divisions between the plurality of segments of the lines are offset from those of the divisions between the plurality of segments of their adjacent lines (fig. 2-5b).

b. Regarding claims 13-16, Ghinovker discloses a semiconductor device comprising a plurality of alignment marks (76, fig. 2-5b) formed over a semiconductor wafer (lines 40-50, col. 4), each of the alignment marks being divided by a micronized line-and-space pattern into a plurality of lines extending along a first direction (76, fig. 2-5b), each of the plural lines being divided into a broken line having a plurality of segments which are arranged in the first direction only (78 of 76, fig. 2-5b), and wherein all of the alignment marks formed in the entire alignment mark area have the same shape so as to generate about the same field image alignment signal (fig. 2-5b). Positions of the divisions between

the plurality of segments of the lines are offset from those of the divisions between the plurality of segments of their adjacent lines (fig. 2-5b). A margin in which the micronized pattern is formed is larger than a margin for a device pattern to be formed on the semiconductor wafer (lines 60-68, col. 4).

PLEASE NOTE: The Examiner notes that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See, e.g., *In re Pearson*, 18 1 USPQ 641 (CCPA); *In re Minks*, 169 USPQ 120 (Bd Appeals); *In re Casey*, 152 USPQ 235 (CCPA 1967); *In re Otto*, 136 USPQ 458, 459 (CCPA 1963); See MPEP §2114. The recitation of “the micronized pattern having a size smaller than a resolution limit of an alignment sensor of field image alignment detecting positions of the alignment marks”, does not distinguish the present invention over Ghinovker ‘833 who teaches the structure as claimed.

Response to Arguments

Applicant's arguments filed 1-17-08 have been fully considered but they are not persuasive.

- a. Applicant argues (pg. 5 of the applicant's arguments) that Ghinovinker's sub-structures are about the same size and pitch as the actual integrated circuits hence the limitation “micronized pattern having a pattern forming margin larger than a pattern forming margin which a device pattern formed over the

semiconductor wafer has" is not met. However, Ghinovinker's sub-structure refers to the finely segmented elements 78 (as admitted by applicant in pg. 4 of applicant's argument). **The plurality of the finely segmented elements, with roughly the same size and pitch of the actual integrated circuits, forms the micronized pattern**, hence the micronized pattern's pattern forming margin is larger than the device pattern margin.

b. Applicant argues that positions of the divisions between the plurality of segments of the lines are offset from those of the divisions between the plurality of segments of their adjacent lines. Examiner notes that such divisions are inherently offset in at least the x direction (fig. 2).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amar Movva whose telephone number is 571-272-9009. The examiner can normally be reached on 7:30 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Amar Movva
Examiner
Art Unit 2891

am

/BRADLEY W BAUMEISTER/

Supervisory Patent Examiner, Art Unit 2891